يتم اجابة السؤال الأول والثاني في الورقة المخصصة لهم ولن يتم تصحيح اي اجابة لهم في كراسة الاجابة الأصلية.

Answer the following questions

Question 1 Choose the correct answer (20 pts):

1. Which of the following addressing mode is **lwi $t3,800** using

   a. Immediate
   b. Indirect
   c. Indexed
   d. Direct

2. Dynamic RAM is used as main memory in a computer system as it

   a. Consumes less power
   e. has higher speed
   b. has lower cell density
   c. needs refreshing circuit

3. The main advantages of register addressing mode are

   f. Flexibility and Speed
   a. Speed and number of address bits
   b. Address bits
   c. All of the above

4. What characteristic of RAM memory makes it not suitable for permanent storage

   a. too slow
   b. unreliable
   c. it is volatile
   d. too bulky

5. The circuit used to store one bit of data is known as

   a. Register
   b. Encoder
   c. Decoder
   d. Flip Flop

6. Which of the following is lowest in memory hierarchy

   a. Cache memory
   b. Secondary memory
   c. Registers
   d. RAM

7. Cache memory acts between

   a. CPU and RAM
   b. RAM and ROM
   c. CPU and Hard Disk
   d. None of these

8. The communication between the components in a microcomputer takes place via the address bus and

   a. I/O bus
   b. Data bus
   c. Address bus
   d. Control lines

9. RAM is called DRAM (Dynamic RAM) when

a. it is always moving around data
b. it requires periodic refreshing
c. it can do several things simultaneously
d. none of the above

10. If multiplexers are used to construct a common bus system for 6 registers of 32 bit each. How many selection inputs of each MUX?
a. one
b. two
c. three
d. none is correct

11. What is the control unit's function in the CPU?
a. To transfer data to primary storage
b. To store program instruction
c. To perform logic operations
d. To decode program instruction

12. Which memory unit has lowest access time?
a. Cache
b. Registers
c. Magnetic Disk
d. Main Memory

13. Cache memory.....
a. has greater capacity than RAM
b. is faster to access than CPU Registers
c. is permanent storage
d. faster to access than RAM

14. FIFO replacement algorithm is not used with ..... mapping function.
a. Direct
b. Associative
c. Set-Associative
d. None of These

15. In which addressing mode the operand is given explicitly in the instruction
a. Absolute
b. Immediate
c. Indirect
d. Direct

16. Which of the following instruction is valid MIPS instruction?
a. lw $t0, $t1($t3)
b. lw $t0, $t1(4)
c. lw $t0, 4($t3)
d. None of These

17. How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes?
a. 2 chips
b. 4 chips
c. 8 chips
d. None of These

18. The line of bus dedicated to move data is.....
a. Data bus
b. Control bus
c. Address bus
d. None of These

19. ..... is the less expensive type of RAM
a. DRAM
b. SRAM
c. PROM
d. None of These

20. What is the register that keeps track of the address of next instruction to be executed?
a. Program Counter
b. Instruction Register
c. Memory Address Register
d. None of These

Question 2 True or False: (10 pts):

1. Operand data can be represented in any order in an instruction. **F**
2. Addressing modes define whether operand values are reside in registers or in memory. **T**
3. In direct addressing mode the operand is given explicitly in the instruction. **F**
4. Write Through technique is used in auxiliary memory for updating the data. **F**
5. A byte is a group of 16 bits **F**
6. FIFO replacement algorithm is used with direct mapping function. **F**
7. A "word" is the natural unit of organization of memory. Different computer types may have different word lengths (in bits). **T**
8. The fetch-decode-execute cycle refers to the process by which data is read from the hard drive and stored in memory. **F**
9. A microoperation is an operation performed with the data stored in registers. **T**
10. Address lines indicate which device has permission to use the bus and for what purpose. **F**

Question 3 (20 pts)

1) What are the 3 main components of a computer?

(3)
- Central Processing Unit
- Memory
- I/O devices

$$\frac{1 \times 2^{20} \times 2^{4}}{2^{9} \times 2^{10} \times 2^{3}} = 2^{4} = 4 \text{ chip}$$

(4) 2) Show how to form 1Mx16 memory module using 512 K X 8 memory chips.

3) Indicate the used addressing mode for each of the following instructions:

(5)
- Move R0,R1 ---------**Register Mode**
- Add R0,5 ---------**Immediate Mode**
- Move R0, [M[AR]] --------- **Indirect Mode**
- Add R0, M[AR] ---------**direct Mode**
- Add A ---------**Accumulator Mode**

(4) 4) What are the differences among direct mapping, associative mapping, and set-associative mapping?

- Direct mapping: The easiest way. Each block of main memory is mapped into only one possible cache line.
- associative mapping: Associative mapping overcome the disadvantages of direct mapping by permitting each main memory block to be loaded into any line of the cache.
- set-associative mapping: Set associative mapping is compromise that exhibits the strengths of both the direct and associative approaches while reducing their disadvantages.

(4) 5) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

6) Tag: 8 Set: 4 bits Word: 7

Question 4 (20 pts)

(3) 1) MIPS 32 is a general purpose processor? What are the means of 32 and general purpose processor?

- General purpose processor: can use for any task.
- 32: instruction length is 32 bits

(3) 2) State the used data types in MIPS 32.

- Byte, Word, Double Word

(6) 3) Write an MIPS 32 program for compute area of a circle.

(3) 4) What is an instruction set? Can we use the same instruction set for all processor types?

- Instructions are the "words" of a computer;Instruction set architecture (ISA) is its vocabulary, No because each processor has its instruction set which is suitable for the processor structure and its memory organization.

(5) 5) A computer employs RAM chips of 256 x8 and ROM chips of 1024x8. The computer system needs 1K bytes of RAM, 2K bytes of ROM. Draw the compete diagram for such system. Show how the address is organized.

(3)

```
Lw   $t0, R
Lw   $t1, PI
mul  $t2, $t0, $t0
mul  $t3, $t2, $t1
sw   $t3, A
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